The buffer memory is an ECC-block-basis buffer memory for storing and reading, on a block-by-block basis, ECC blocks to be processed in parallel.

The storing means for storing mid-term results of an error detecting process generated by the error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis.

In the system control means, the means-basis ECC block pipeline processing notification sub means transmits ECC blocks which have been subjected to error correction downstream; stores ECC blocks to be processed next to the ECC-block-basis buffer memory; and makes the storage known to the bus control means, the syndrome calculating means, the error detecting means, and the error correcting means.

The means-basis ECC block code word recognition sub means selects code words of the ECC blocks to be processed, in accordance with the contents stored in the ECC-block-and-code word-division storing means, in controlling a data transfer from the bus control means to the syndrome calculating means, to the error detecting means, and to the error correcting means for error detection and error correction; in controlling the error correction done by the error correcting means; in controlling writing of error-corrected data to the ECC-block-basis buffer memory done by the bus control means; in storing mid-term results to the ECC-block-and-code word-division storing means by the error detecting means.

The ECC block code word recognition sub means in sub means-basis

pipeline processing makes the first error detecting sub means, the even-numbered error correction sub means, the odd-numbered error correction sub means, the number-of-times control sub means, and the DMA transfer instruction sub means in case equipped in the system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in the ECC-block-basis buffer memory, and further makes these same sub means contained in the system control means recognize the ECC blocks and the code words which are to be processed therein.

In order to facilitate the pipeline processing and the use of the mid-term results of error detection, the system control means has a conceptual list of each ECC block, each sector and each code word in each ECC block to be processed.

While in the error correction devices of the aspects 1, 2, 5, 6, 7, 8, 9, 10, and 11, the pipeline processing of the aspects 12-15 makes data be stored in descending order of ECC blocks in the buffer memory and transmitted downstream block by block after error correction is done as a rule. In contrast, in the aspects 20-23, several ECC blocks are collectively stored in the buffer memory in descending order and collectively transmitted downstream after error correction.

The collective data transfer is useful, for example, in a video-on-demand system where image data are transmitted in extremely short time units in order to transmit the same movie or the like to as many viewers as possible approximately at the same time. To be more specific, error correction is executed scene by scene, and if complete error correction

is impossible, the CPU can correct data of a scene by extrapolation with the data prior to and subsequent to the scene.

The collective data transfer is also useful when discrete data for one scene is subjected to error correction in high-speed reproduction for retrieval. In this case, it goes without saying that data for one scene are recognized in compliance with recording in CPU or the like or communication regulations (protocol)(for example, EOP signals).

In the error correction devices of the aspects 20-23, the mid-term results of previous error calculation are used in ECC units in and after the second time error correction. In contrast, in the aspects 24-27, the mid-term results are used in predetermined data units such as one sector at a time or one sector group at a time. Therefore, the aspects 24-27 provide the aspects 23-29 with the same advantages and effects that the aspects 16-19 provide to the aspects 12-15.

The aspect 28 relates to an error correction device which performs error correction for data in ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of code words in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to error correction, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory.

The first syndrome calculating means performs syndrome calculation